CLAIMS

What is claimed is:

1. A variable length instruction pipeline comprising:

a first pipeline stage;

a first expansion stage coupled to the first pipeline stage; and

a second pipeline stage coupled to the first pipeline stage and the first expansion stage, wherein the second pipeline stage is configured to selectively receive instructions from the first pipeline stage or the first expansion stage.

2. The variable length instruction pipeline of Claim 1, further comprising a multiplexer coupled between the first expansion stage and the second pipeline stage and between the first pipeline stage and the second pipeline stage.

3. The variable length instruction pipeline of Claim 1, further comprising a second expansion stage coupled to the first pipeline stage and the first expansion stage and wherein the first expansion stage is configured to selectively receive instructions from the first pipeline stage or the second expansion stage.

4. The variable length instruction pipeline of Claim 3, further comprising a multiplexer coupled between the second expansion stage and the first expansion stage and between the first pipeline stage and the first expansion stage.

5. The variable length instruction pipeline of Claim 1, further comprising a third pipeline stage coupled to the second pipeline stage.

6. The variable length instruction pipeline of Claim 1, wherein the first pipeline stage is part of an instruction fetch and decode unit.

7. The variable length instruction pipeline of Claim 6, wherein the instruction fetch and issue unit further comprises an instruction fetch stage coupled to the first pipeline stage.

8. The variable length instruction pipeline of Claim 1, wherein the second pipeline stage is a decode stage.

9. The variable length instruction pipeline of Claim 1, wherein the variable length instruction pipeline is configured to process integer instructions.

10. The variable length instruction pipeline of Claim 1, wherein the first pipeline stage issues an instruction to the first expansion stage when the second pipeline stage is full.

11. A method of avoiding pipeline stalls using a variable length instruction pipeline having a first pipeline stage, a first expansion stage, and a second pipeline stage, the method comprising:

issuing a first instruction from the first pipeline stage to the second pipeline stage if the second pipeline stage can accept the first instruction;

issuing the first instruction to the first expansion stage when the second pipeline stage can not accept the first instruction.

12. The method of Claim 11, further comprising issuing a second instruction to a second expansion stage when the first expansion stage retains the first instruction.

13. The method of Claim 12, further comprising issuing the second instruction from the second expansion stage to the first expansion stage when the first expansion stage can receive the second instruction.

14. The method of Claim 13, further comprising issuing a third instruction from the first pipeline stage to the first expansion stage when the second instruction leaves the first expansion stage.

15. The method of Claim 15, further comprising issuing a fourth instruction from the first pipeline stage to the second pipeline stage when the third instruction leaves the second pipeline stage.

16. The method of Claim 11, further comprising issuing a second instruction from the first pipeline stage to the first expansion stage when the first instruction leaves the first expansion stage.

17. The method of Claim 16, further comprising issuing a third instruction from the first pipeline stage to the first pipeline stage when the second instruction leaves the first pipeline stage.

18. A variable length instruction pipeline comprising:

a first pipeline stage;

a first expansion stage coupled to the first pipeline stage; and

a second pipeline stage coupled to the first pipeline stage and the first expansion stage,

wherein the first pipeline stage is configured to issue a first instruction into the first expansion stage when the second pipeline stage can not receive an instruction.

19. The variable length instruction pipeline of Claim 18, further comprising a multiplexer coupled between the first expansion stage and the second pipeline stage and between the first pipeline stage and the second pipeline stage.

20. The variable length instruction pipeline of Claim 18, further comprising a second expansion stage coupled to the first pipeline stage and the first expansion stage and wherein the first pipeline stage is configured to issue a second instruction to the second expansion stage when the first instruction is in the first expansion stage.

21. The variable length instruction pipeline of Claim 20, further comprising a multiplexer coupled between the second expansion stage and the first expansion stage and between the first pipeline stage and the first expansion stage.

22. The variable length instruction pipeline of Claim 18, further comprising a third pipeline stage coupled to the second pipeline stage.

23. The variable length instruction pipeline of Claim 18, wherein the first pipeline stage is part of an instruction fetch and issue unit.